PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: Jae-Eun LIM, et al.

Serial No.: New Application Group Art Unit: Not Yet Assigned

Filed: December 16, 2003 Examiner: Not Yet Assigned

Title: METHOD FOR MANUFACTURING SHALLOW TRENCH ISOLATION IN

SEMICONDUCTOR DEVICE

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

December 16, 2003

Sir:

As a means of complying with the duty of disclosure under 37 CFR §1.56, and in accordance with 37 CFR §§1.97 and 1.98, Applicant(s), through the undersigned attorney, submits this Information Disclosure Statement. The patents, publications or other information submitted herewith are listed on the attached Form PTO-1449 and copies are attached.

In accordance with 37 CFR §1.97(b)(1) or (2), this Information Disclosure Statement is being filed either within three months of the filing date of the above-identified application, or within three months of the date of entry into the national stage of the above-identified application as set forth in 37 CFR §1.491. Accordingly, no fee is required.

Respectfully submitted,

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Atty. Dkt. No.: P69388US0 YSH:dj

Information Disclosure Statement

New U.S. Patent Application for METHOD FOR MANUFACTURING SHALLOW TRENCH ISOLATION IN SEMICONDUCTOR DEVICE Our Ref. No.: P03H8032/US/gy

Reference No.:

- (1) US Patent No. 6,177,333
- (2) US Patent No. 6,162,700

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LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT

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^{*} EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).